

### FEATURES

- Ultra-low Phase Jitter, 50fs typical
- LVCMOS output
- Supply voltage 1.8, 2.5 or 3.3 Volts
- Frequency stability from  $\pm 25$ ppm over  $-40^{\circ}$  to  $+85^{\circ}\text{C}$
- Available in three standard SM packages.

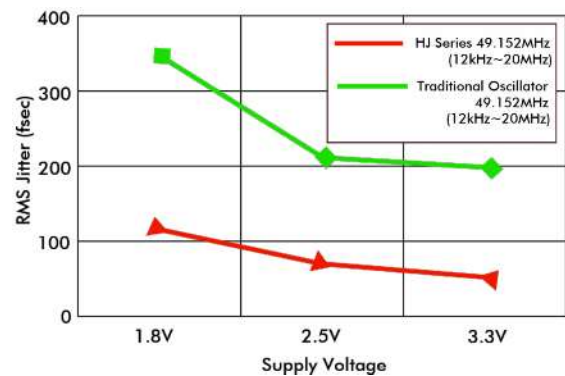


### GENERAL SPECIFICATION

Model (Output Logic)	"HJ Series LVCMOS		
Type	EQHJ32	EQHJ53	EQHJ57
Dimensions	3.2 x 2.5 x 1.0mm	5.0 x 3.2 x 1.2mm	7.0 x 5.0 x 1.4mm
Frequency Range	5.0MHz to 50.0MHz	5.0MHz to 50.0MHz	5.0MHz to 50.0MHz
Supply Voltage $V_{DD}$	1.8V $_{DD} \pm 10\%$ Voltage code is "18"	2.5V $_{DD} \pm 10\%$ Voltage code is "25"	3.3V $_{DD} \pm 10\%$ Voltage Code is "3"
Current Consumption	3mA typical, 5mA maximum	4.7mA typical, 7mA maximum	7mA typical, 10mA maximum
Output Logic "HIGH," "1"	1.62V (minimum)	2.25 (minimum)	2.97V (minimum)
Output Logic "LOW," "0"	0.18V (maximum)	0.25V (maximum)	0.33V (maximum)
Rise Time ( $T_R$ )/Fall Time ( $T_F$ )	5.0ns typical, 10ns maximum	2.0ns typical, 10ns maximum	1.5ns typical, 10ns maximum
Measured between 10% - 90% of $V_{DD}$ , (CL = 15pF)			

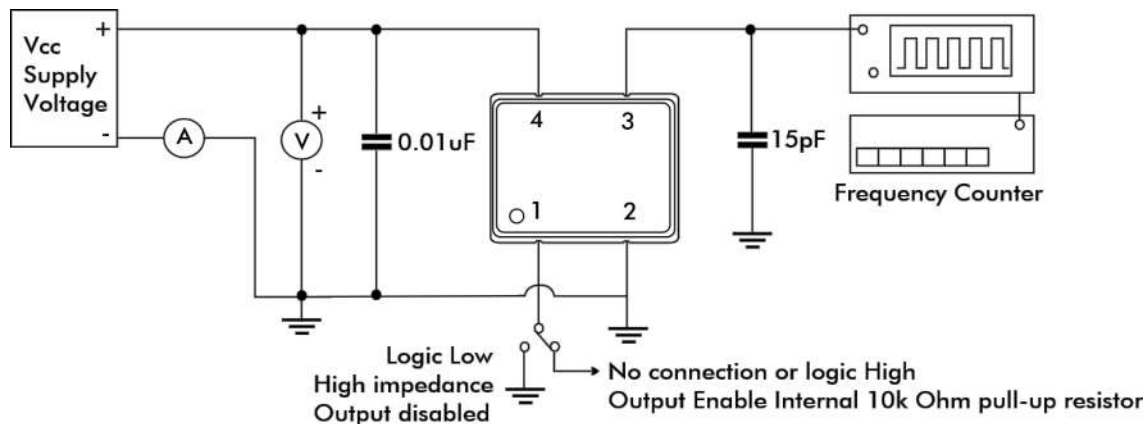
Supply Voltage vs. Freq. Stability:	$\pm 1.0$ ppm (maximum)
Load:	15pF (CMOS)
Start-up Time:	0.8ms typical, 5.0ms max.
Duty Cycle:	50% $\pm 5\%$ (Measured at 50% $V_{DD}$ )
Tristate Function on Pad no. 1:	High Enable
Enable/Disable Time	Enable: 1ms max. Disable: 200ns max.
Storage Temperature:	$-55^{\circ}$ to $+150^{\circ}\text{C}$
Ageing at $T_a = 25^{\circ}\text{C}$ :	$\pm 3$ ppm max. in first year $\pm 2$ ppm max. per year thereafter
RMS Phase Jitter (at 49.152MHz):	48fs typical at 3.3V $_{DD}$ 118fs typical at 1.8V $_{DD}$

HJ Series vs. Traditional Osc. Phase Jitter



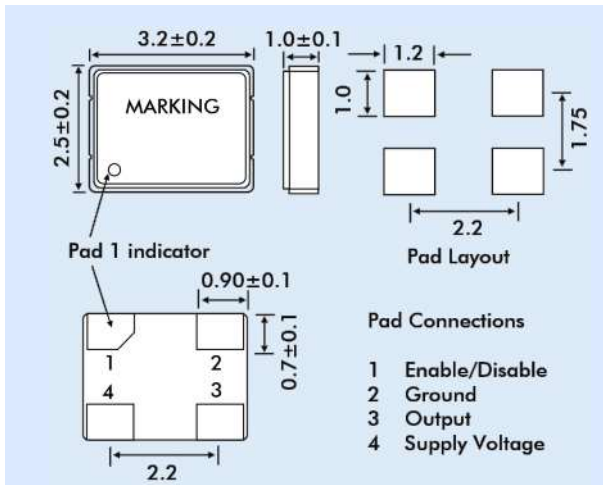
SSB Phase Noise	Offset	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz	10MHz	20MHz
49.152MHz, 3.3V	dBC/Hz (typ.)	-91	-126	-141	-153	-166	-171	-172	-174
49.152MHz, 1.8V	dBC/Hz (typ.)	-97	-120	-132	-146	-159	-164	-164	-165

### CMOS TEST CIRCUIT

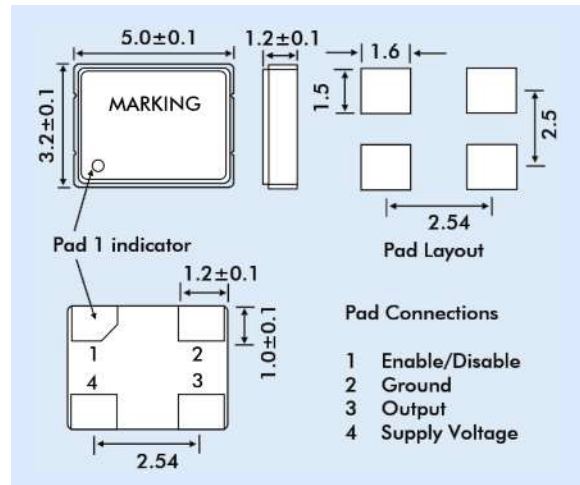


### OUTLINES & DIMENSIONS

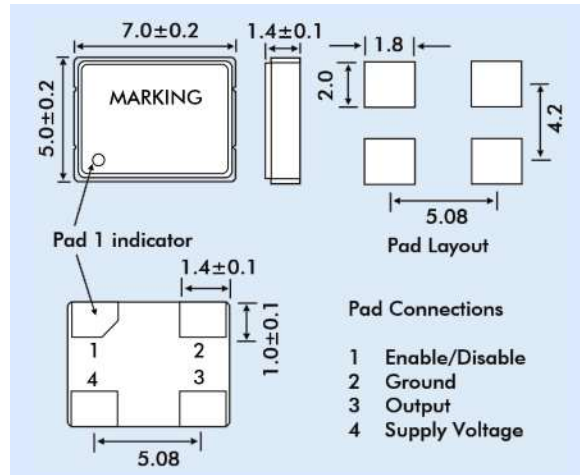
#### EQHJ32



#### EQHJ53



#### EQHJ57



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### PART NUMBERING

(1)	(2)	(3)	(4)	(5)
Supply Voltage	Holder Type	Frequency Stability	T	Centre Frequency

Examples	(1)	18	EQHJ32	B	T	25.000
	(2)	25	EQHJ53	C30	T	10.000
	(3)	3	EQHJ57	E	T	49.152

Ex.(1): 18HJ32 - BT - 25.000 (1.8V, EQHJ32 package, Tristate on pin 1, ±50ppm -10° to +70°C, 25.000MHz.  
 Ex.(2): 25EQHJ53 - C30T - 10.000 (2.5V, EQHJ53 package. Tristate on pin 1, ±30ppm -10° to +70°C, 10.000MHz.  
 Ex.(3): 3EQHJ57 - ET - 49.152 (3.3V, EQHJ57 package, Tristate on pin1, ±50ppm over -40° to +85°C, 49.152MHz.

(1)	Supply Voltage, "18" for +1.8V, "25" for +2.5V, "3" for +3.3V	
(2)	Holder Type - see above	
(3)	-10° ~ +70°C	"A" ±25ppm, "B" ±50ppm, "C" ±100ppm If non-standard enter stability after "C". Examp. "C15" = ±15ppm over -10°~+70°C
	-40° ~ +85°C	"D" ±25ppm, "E" ±50ppm, "F" ±100ppm If non-standard enter stability after "I". Examp. "I30" = ±30ppm over -40°~+85°C
(4)	"T" for Tristate function	
(5)	Frequency in MHz	